SystemVerilog Coding Standard for Synthesizable FPGA code

# Rule 1-1: Variable identifier name convention

The variable identifier name has a prefix, which specifies its data type and range. The prefix is comprised of a two-character identifier <xx> specific to the data type followed by a number <n> specifying the number of bits for logic data types:

<xx><n><identifier>

|  |  |  |
| --- | --- | --- |
| Data type | <xx> | <n> |
| logic | ul | Arbitrary |
| logic signed | sl | Arbitrary |

Examples:

logic ul1Enable

logic [7:0] ul8UnsignedData

logic signed [15:0] sl16SignedData

# Rule 1-2: Port identifier name convention

The port identifier name follows the variable name convention [Rule 1-1] with a prefix, which specifies the port direction. The prefix is comprised of the character ‘p’ followed by a single character to specify the direction of the port:

p<x><identifier>

|  |  |
| --- | --- |
| Direction | p<x> |
| input | pi |
| output | po |
| inout | px |

Examples:

input logic piul1Clk

output logic [7:0] poul8Status

inout logic [15:0] pxul16DIO

# Rule 1-3: Interface identifier declaration

The interface identifier has a prefix ‘tI’:

Example:

Interface tIDataBus (…) … endinterface